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METHOD TO ALTER CHALCOGENIDE GLASS FOR IMPROVED SWITCHING CHARACTERISTICS

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METHOD TO ALTER CHALCOGENIDE GLASS FOR IMPROVED SWITCHING CHARACTERISTICS

FIELD OF THE INVENTION

[0001] The present invention relates to the field of random access memory (RAM) devices formed using a resistance variable material, and in particular to a resistance variable memory element having improved switching characteristics.

BACKGROUND OF THE INVENTION

[0002] A well known semiconductor component is semiconductor memory, such as a random access memory (RAM). RAM permits repeated read and write operations on memory elements. Typically, RAM devices are volatile, in that stored data is lost once the power source is disconnected or removed. Non-limiting examples of RAM devices include dynamic random access memory (DRAM), synchronized dynamic random access memory (SDRAM) and static random access memory (SRAM). In addition, DRAMS and SDRAMS also typically store data in capacitors which require periodic refreshing to maintain the stored data.

[0003] In recent years, the number and density of memory elements in memory devices have been increasing. Accordingly, the size of each element has been shrinking, which in the case of DRAMs also shortens the element's data holding time. Typically, a DRAM memory device relies on element capacity for data storage and receives a refresh command in a conventional standardized cycle, about every 100 milliseconds. However, with increasing element number and density, it is becoming more and more difficult to refresh all memory elements at least once within a refresh period. In addition, refresh operations consume power.

[0004] Recently resistance variable memory elements, which includes programmable conductor memory elements, have been investigated for suitability as semi-volatile and non-volatile random access memory elements. Kozicki et al. in

U.S. Patent Nos. 5,761,115; 5,896,312; 5,914,893; and 6,084,796, discloses a programmable conductor memory element including an insulating dielectric material formed of a chalcogenide glass disposed between two electrodes. A conductive material, such as silver, is incorporated into the dielectric material. The resistance of the dielectric material can be changed between high resistance and low resistance states. The programmable conductor memory is normally in a high resistance state when at rest. A write operation to a low resistance state is performed by applying a voltage potential across the two electrodes. The mechanism by which the resistance of the element is changed is not fully understood. In one theory suggested by Kozicki et al., the conductively-doped dielectric material undergoes a structural change at a certain applied voltage with the growth of a conductive dendrite or filament between the electrodes effectively interconnecting the two electrodes and setting the memory element in a low resistance state. The dendrite is thought to grow through the resistance variable material in a path of least resistance.

[0005] The low resistance state will remain intact for days or weeks after the voltage potentials are removed. Such material can be returned to its high resistance state by applying a reverse voltage potential between the electrodes of at least the same order of magnitude as used to write the element to the low resistance state. Again, the highly resistive state is maintained once the voltage potential is removed. This way, such a device can function, for example, as a resistance variable memory element having two resistance states, which can define two logic states.

[0006] One preferred resistance variable material comprises a chalcogenide glass. A specific example is germanium-selenide (Ge_xSe_{100-x}) comprising silver (Ag). One method of providing silver to the germanium-selenide composition is to initially form a germanium-selenide glass and then deposit a thin layer of silver upon the glass, for example by sputtering, physical vapor deposition, or other known technique in the art. The layer of silver is irradiated, preferably with electromagnetic energy at a wavelength less than 600 nanometers, so that the energy passes through the silver and to the silver/glass interface, to break a chalcogenide bond of the

chalcogenide material such that the glass is doped with silver. Silver may also be provided to the glass by processing the glass with silver, as in the case of a silver-germanium-selenide glass. Another method for providing metal to the glass is to provide a layer of silver-selenide on a germanium-selenide glass.

[0007] The mean coordination number of the glass defines the tightness of the glass matrix. If the chalcogenide glass matrix is tight, then a larger resistance change is inhibited when a memory element switches from an on to an off state. On the other hand, if the chalcogenide glass matrix is looser (more open), then a larger resistance change is more easily facilitated. Accordingly, glasses having an open matrix, e.g., a larger resistance change, require a longer time to write when reprogrammed to the low resistance state. Conversely, glasses having a tight matrix, e.g. inhibiting large resistance changes, will write to the low resistance state faster.

[0008] Although glasses having an open matrix may comprise silver, it would be advantageous to use a silver containing glass having a tight matrix. However, a disadvantage of using a tight matrix glass is that it is difficult to provide silver to the glass and achieve good switching.

[0009] Silver can be directly incorporated into a resistance variable material having an open matrix, such as $Ge_{20}Se_{80}$ or $Ge_{23}Se_{77}$ to form silver-selenide within the Ge_xSe_{100-x} backbone. The Ge_xSe_{100-x} backbone, however, is lacking the Se that went into forming the silver-selenide. The remaining glass backbone does not have a mean coordinator number corresponding to a tight matrix, like $Ge_{40}Se_{60}$. As a consequence, there is greater Ag mobility causing a larger resistance change when a memory element is programmed back to its high resistance state.

[0010] It would be desirable to have a chalcogenide glass memory element comprising silver and which also has a tight glass matrix to inhibit metal migration thus allowing the memory element to retain memory longer and inhibiting a large

resistance change when the memory element is programmed back to its high resistance state.

BRIEF SUMMARY OF THE INVENTION

[0011] In its structure aspect, the invention provides a metal containing resistance variable material having a tighter more rigid glass matrix, which exhibits improved switching characteristics and data retention.

[0012] The invention also provides a Ge_xSe_{100-x} glass memory element incorporating silver therein and which has a tighter more rigid glass matrix.

[0013] In its method aspect, the invention provides a method in which a metal is incorporated into a resistance variable material and then the metal containing resistance variable material is annealed to provide a tighter more rigid glass matrix.

[0014] In a more specific aspect, the invention provides a method in which a silver-germanium-selenide glass is annealed to provide a tighter more rigid glass matrix.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] These and other features and advantages of the invention will be better understood from the following detailed description, which is provided in connection with the accompanying drawings.

[0016] FIG. 1 illustrates a process according to an embodiment of the present invention;

[0017] FIG. 2 is a cross-sectional view of a resistance variable memory element constructed in accordance with the process of FIG. 1; and

[0018] FIG. 3 illustrates a computer system having one or more memory devices that contains resistance variable memory elements according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0019] In the following detailed description, reference is made to various specific structural and process embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that other embodiments may be employed, and that various structural, logical and electrical changes may be made without departing from the spirit or scope of the invention.

[0020] The term "substrate" used in the following description may include any supporting structure including but not limited to a semiconductor substrate that has an exposed substrate surface. Structure should be understood to include silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is made to a substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation.

[0021] The term "silver" is intended to include not only elemental silver, but silver with other trace metals or in various alloyed combinations with other metals as known in the semiconductor industry, as long as such silver alloy is conductive, and as long as the physical and electrical properties of the silver remain unchanged.

[0022] The term "silver-selenide" is intended to include various species of silver-selenide, including some species which have a slight excess or deficit of silver, for instance, Ag_2Se, $Ag_{2+x}Se$, and $Ag_{2-x}Se$.

[0023] The term "semi-volatile memory device" is intended to include any memory device which is capable of maintaining its memory state after power is removed from the device for a prolonged period of time. Thus, semi-volatile memory devices are capable of retaining stored data after the power source is disconnected or removed. The term "semi-volatile memory device" as used herein includes not only semi-volatile memory devices, but also non-volatile memory devices.

[0024] The term "resistance variable material" is intended to include chalcogenide glasses, and chalcogenide glasses comprising a metal, such as silver. For instance the term "resistance variable material" includes silver doped chalcogenide glasses, silver-germanium-selenide glasses, and chalcogenide glasses comprising a silver selenide layer.

[0025] The term "resistance variable memory element" is intended to include any memory element, including programmable conductor memory elements, semi-volatile memory elements, and non-volatile memory elements which exhibit a resistance change in response to an applied voltage.

[0026] The present invention relates to a method of forming a resistance variable memory element having improved switching characteristics and to the resulting memory element.

[0027] Applicants have discovered that the tightness and hence rigidity of the glass matrix of a chalcogenide glass used in a resistance variable memory element determines the speed at which a memory elements switches. For instance, if the memory element erases to a larger or higher resistance, the memory element will write more slowly than if the memory element erases to a smaller or lower resistance.

The tightness of the glass matrix is generally characterized by the mean coordination of the glass. Boolchand et al. in *Onset of Rigidity in Steps in Chalcogenide Glass*, Properties and Applications of Amorphous Materials, pp. 97-132, (2001), the disclosure of which is incorporated by reference herein, observes a floppy to rigid transition in Ge_xSe_{100-x} glasses that occurs when x = 0.23 (x being the germanium molar concentration). Raman scattering and Temperature Modulated Differential Scanning Calorimetric (MDSC) measurements have shown that a stiffness threshold occurs at a mean coordination number of r = 2.46. Thus a glass having a stoichiometry greater than about $Ge_{23}S_{77}$ or a mean coordination number of about 2.46 or greater is rigid. Glasses characterized as rigid are stiff and have a rigid network or closed matrix type structure. Lower rigidity glasses, i.e., glasses having an open matrix, include glasses having a stoichiometric range of about $Ge_{20}Se_{80}$ to about $Ge_{23}Se_{77}$.

[0028] Applicants have further discovered that glasses having a rigid network structure inhibit larger resistance changes, resulting in memory elements which can be reprogrammed to a low resistance state relatively faster, thusly having shorter write cycles and better switching characteristics.

[0029] In accordance with the invention, silver is incorporated into a lower rigidity glass, such as for example $Ge_{20}Se_{80}$ to $Ge_{23}Se_{77}$. Then the silver containing glass is annealed, preferably by heating, to produce a more rigid glass. The silver containing glass is also preferably annealed in the presence of oxygen. Annealing drives off a portion of the selenium in the glass and raises the germanium to selenium ratio. It is known that the higher the germanium to selenium ratio, the more tightly packed the glass matrix and the more rigid the structure. Accordingly, a memory element formed of the annealed glass switches faster than conventionally formed glasses.

[0030] Typical temperatures for packaging of memory elements are of about 170°C to about 190°C (e.g., for encapsulation) and can be as high as 230°C

(e.g., for wire bonding). Typical processing steps during the fabrication of resistance variable memory elements, for example photoresist and/or nitride deposition processes, can also take place at temperatures of about 200°C. Generally acceptable chalcogenide glass compositions for resistance variable memory elements have a glass transition temperature, which is about or higher than the highest packaging and/or processing temperatures used during the formation of the memory device or of the packaging of the memory device itself. For instance, $Ge_{40}Se_{60}$ glass has a bulk material glass transition temperature of about 347°C. It is believed that the thin-film, as opposed to the bulk material, transition temperature of the backbone may be slightly higher than the transition temperature of the bulk resistance variable material. Accordingly, to prevent glass transition, the resistance variable material thin-film is annealed at temperatures close to or slightly below the thin-film glass transition temperature of the resistance variable material.

[0031] FIG. 1 illustrates a process 100 according to an exemplary embodiment of the method of the invention. While FIG. 2 depicts one exemplary structure formed in accordance with the process of FIG. 1.

[0032] Refer now to FIG. 1 at process segment 110 a first electrode is formed over a substrate assembly. The material used to form the electrode can be selected from a variety of conductive materials, for example, tungsten, nickel, tantalum, titanium, titanium nitride, aluminum, platinum, or silver, among many others.

[0033] Next, at process segment 120, an insulating layer is formed in contact with the first electrode. This and any other subsequently formed insulating layers may be formed of a conventional insulating nitride or oxide, among others. The present invention is not limited, however, to the above-listed materials and other insulating and/or dielectric materials known in the industry may be used. The insulating layer may be formed by any known deposition methods, for example, by

sputtering, chemical vapor deposition (CVD), plasma enhanced CVD (PECVD) or physical vapor deposition (PVD), among others.

[0034] In the next process segment 130, the insulating layer is etched to form an opening, which exposes the first electrode. Subsequently, in process segment 140, a resistance variable material is deposited into the opening. The resistance variable material is deposited in such a manner so as to contact the first electrode. In an exemplary embodiment, the resistance variable material is a germanium-selenide glass. The germanium-selenide glass composition is of a relatively low rigidity, such as one having a Ge_xSe_{100-x} stoichiometry of from about $Ge_{20}Se_{80}$ to about $Ge_{23}Se_{77}$. The resistance variable material may be deposited by any known deposition methods, for example, by sputtering, chemical vapor deposition (CVD), plasma enhanced CVD (PECVD) or physical vapor deposition (PVD). The resistance variable material may be formed over the first electrode to dimensions (i.e., length, thickness, and width) suitable to produce desired electrical characteristics of the memory element.

[0035] In process segment 150, a metal, such as silver, is incorporated into the resistance variable material. For a Ge_xSe_{100-x} glass where x = 20 to 23, silver (Ag) is preferably incorporated into the resistance variable material. One technique for incorporating silver into a germanium-selenide glass is by processing the glass with silver to form silver-germanium-selenide. Another technique for incorporating silver into a resistance variable material is doping. The resistance variable material may be doped by first coating the material with a layer of silver, for example, by sputtering, and then driving the silver into the material with UV radiation. Alternatively, the silver can be co-sputtered with the resistance variable material composition to produce a doped resistance variable material. Silver may also be incorporated into the resistance variable material by providing silver as a separate layer, for instance, a silver-selenide (silver-selenide) layer provided on a germanium-selenide glass.

[0036] In process segment 160, the resistance variable material backbone is annealed. The backbone may be annealed at this point in processing, preferably by heating the substrate assembly. However, the backbone may be annealed at any suitable time during fabrication of the resistance variable memory element. A suitable annealing temperature is an elevated temperature close to or slightly below the thin-film glass transition temperature of the resistance variable material. A preferred range of elevated annealing temperatures for a germanium-selenide glass backbone, is from about 200°C to about 330°C. The substrate is preferably annealed for about 5 to about 15 minutes, and more preferably about 10 minutes. The substrate is also preferably annealed in an atmosphere comprising oxygen. Annealing the substrate drives off some selenium from the germanium-selenide glass. The loss of selenium in the glass backbone changes the stoichiometry of the glass increasing the relative amount of germanium and providing a more rigid glass.

[0037] After annealing, in process segment 170, a second metal electrode is formed in contact with the silver-germanium-selenide glass. As noted, the annealing step can be performed at any time during the fabrication and/or packaging of the memory element, provided suitable annealing temperatures as noted above are present.

[0038] The structure produced by one implementation of the exemplary process described with reference to FIG. 1 is shown in FIG. 2 in the context of a random access memory device. However, it should be understood that the invention may be used in other types of memory devices. Also, other embodiments may be used and structural or logical changes may be made to the described and illustrated embodiment without departing from the spirit or the scope of the present invention.

[0039] FIG. 2 illustrates an exemplary construction of a resistance variable memory element. A resistance variable memory element 10 in accordance with the present invention is generally fabricated over a semiconductor substrate 62 and

comprises a first insulating layer 60 formed over a substrate 62 in and on which may be fabricated access circuitry for operating a resistance variable memory element as part of a memory array of such elements. The insulating layer 60 contains a conductive plug 61. In accordance with process segment 110, a first metal electrode 52 is formed within a second insulating layer 53 provided over the insulating layer 60 and plug 61. In accordance with process segment 120, a third insulating layer 68 is formed over the first electrode 52 and second insulating layer 53. In accordance with process segment 130, an etched opening is provided for depositing a chalcogenide glass 58 in the opening of the third insulating layer 68.

[0040] Following through to process segment 140, the chalcogenide glass 58 is deposited in the opening and in contact with the first electrode 52. In accordance with process segment 150, a metal, preferably silver, is incorporated into the chalcogenide glass. As described, the glass may be a silver-germanium-selenide glass, or the metal may be provided in numerous different ways, including incorporation into the glass by doping the glass with a metal dopant. The metal dopant preferably comprises silver.

[0041] In accordance with process segment 160, the glass backbone 66 is subsequently annealed to drive off selenium from the silver-germanium-selenide glass and form a more rigid glass structure. Next, according to process segment 170, a second metal electrode 54 is formed in contact with the silver-germanium-selenide glass 58.

[0042] The third insulating layer 68 may be formed, for example, between the first electrode 52 and the second electrode 54 of any suitable insulator, for example a nitride, an oxide, or other insulator. The third insulating layer 68 may be formed by any known deposition method, for example, by sputtering, chemical vapor deposition (CVD), plasma enhanced CVD (PECVD) or physical vapor deposition (PVD), among others. The third insulating layer 68 may comprise an insulating material that provides a diffusion barrier for metals, such as silver. A

preferred insulating material is silicon nitride, but those skilled in the art will appreciate that there are other numerous suitable insulating materials for this purpose. The thickness T of the third insulating layer 68 and chalcogenide glass 58 is in the range of from about 100 Angstroms to about 10,000 Angstroms and is preferably about 500 Angstroms.

[0043] As noted, the chalcogenide glass 58 is preferably a germanium-selenide composition comprising silver and having a Ge/Se stoichiometry of from about $Ge_{20}Se_{80}$ to about $Ge_{23}Se_{77}$. However, the invention may also be carried out with other chalcogenide glasses having other metals incorporated therein, as long as the glass is annealed to increase its rigidity.

[0044] The first electrode 52 may also be electrically connected to a source/drain region 81 of an access transistor 83, which is fabricated within and on substrate 62. Another source/drain region 85 may be connected by a bit line plug 87 to a bit line of a memory array. The gate of the transistor 83 may be part of a word line which is connected to a plurality of resistance variable memory elements just as the bit line 93 may be coupled to a plurality of resistance variable memory elements through respective access transistors. The bit line 93 may be formed over a fourth insulating layer 91 and may be formed of any conductive material, for example, a metal. As shown, the bit line 93 connects to the bit line plug 87, which in turn connects with access transistor 83.

[0045] Although FIG. 2 illustrates the formation of only one resistance variable memory element 10, it should be understood that the present invention contemplates the formation of any number of such resistance variable memory elements, which can be formed within one or more memory element arrays.

[0046] The above description and drawings are only to be considered illustrative of exemplary embodiments, which achieve the features and advantages of the present invention. Modification and substitutions to specific process conditions

and structures can be made without departing from the spirit and scope of the present invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.